# Power, Speed and Density Trade-offs in Modern FPGA Architectures: A Review for Optimization Techniques

**Engr.Dilip kumar.A.Ramnani[1]*, Dr.Khalil ur Rehman Dayo[2] , Dr. Muhammad Amir[3]**

[1]Department of Electronic Engineering, Dawood University of Engneering & Technology Karachi, Pakistan
dilip.ramnani@duet.edu.pk

[2]Department of Electronic Engineering, Mehran University of Engineering &Technology Jamshoro, Pakistan
krdayo@yahoo.com

[3]Department of Electronic Engineering, Sir Syed University of Engineering & Technology Karachi, Pakistan
muaamir5@gmail.com

**Abstract:** FPGAs are an arrangement of gates that can be reprogrammed or reconfigured. In FPGA, Logic functions are usually implemented by Logic Blocks, Programmable Routing, and Input-output Blocks. FPGAs are more adaptable than ASICs but they are relatively larger in size, slower and consume more power because of routing which uses almost 90% of the overall area in FPGA. Our work explains detailed analysis of the existing techniques addressing different issues such as; routing, mapping, cluster, optimization, and energy efficiency related to FPGA power, speed delay and area density. By analyzing different FPGAs architecture techniques, we revealed that low power consumption and fast speed can be achieved by designing FPGA with large cluster size, however efficient area can be achieved by designing FPGA with small cluster size. Lookup table with four input gives most effective tradeoff between Power, speed and Area. This paper also suggests the latest area for optimizing the power, speed delay and area density for different FPGA architecture.

**Keywords:** Field Programmable Gate Arrays (FPGAs), Programmable logic blocks, Programmable routing, I/O blocks, Look-up-Table (LUT), Power Consumption.

## 1. Introduction

Field Programmable Gate Arrays (FPGAs) are different than any other microprocessor or microcontroller devices. In (FPGAs), no processor to run software on until users design it. These configurable and their design can be created using different HDL programming languages. Best features of Application Specific Integrated Circuits (ASICs) and Processor-based systems are merged in FPGAs. This is the reason why FPGAs are implemented in industries. These feature are:

- Provides faster response with dedicated functionality
- Powerful Digital Signal Processors.
- No cost of re-design as FPGAs are field upgradable.
- Provides custom functionality of hardware with reliability.
- Fast Prototyping without fabrication process used in custom ASIC designing.

A modern FPGA architecture is shown in Figure.1 that comprises of three sections:1) Configurable logic block (CLB) 2) Routing Resources consist of interconnect wires and switch matrix and 3) Input/outputs bank or I/O block. Along with the FPGA architecture, the optimization techniques are also equally important for the modern aspect of FPGA. An FPGA architecture with optimization techniques and their related parameters are discussed next.

### 1.1. Configurable logic block

Functionality of mapping circuit is implemented by CLBs, where connection between logic element is accomplished by routing resources [1]. Structure and granularity of Logic block are crucial parameters regarding FPGA performance. More logic blocks will be required to implement specific logic if blocks are fine-grained as a result more routing space is needed to provide connection between blocks. However if coarse-grained blocks are used then most of logic functions are not used frequently due to this area is wasted [2].

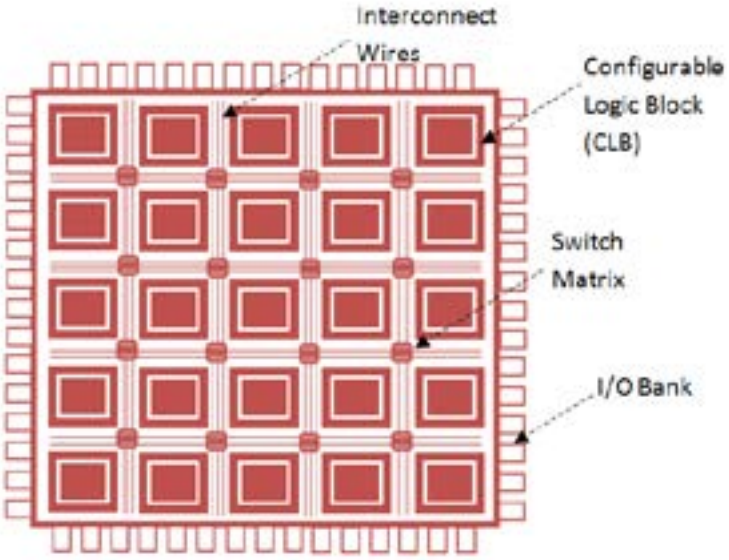


**Fig.1:** Basic Structure of FPGA [1]

The problem of coarse grained and fine grained tradeoff in logic blocks can be overcome by using LUT based CLBs which comprises of Basic Logic Elements (BLE), shown in Figure.2. A single BLE contains LUT, Flip-Flop and Multiplexer. Four to Ten BLEs are used in a single cluster modern FPGAs [6].

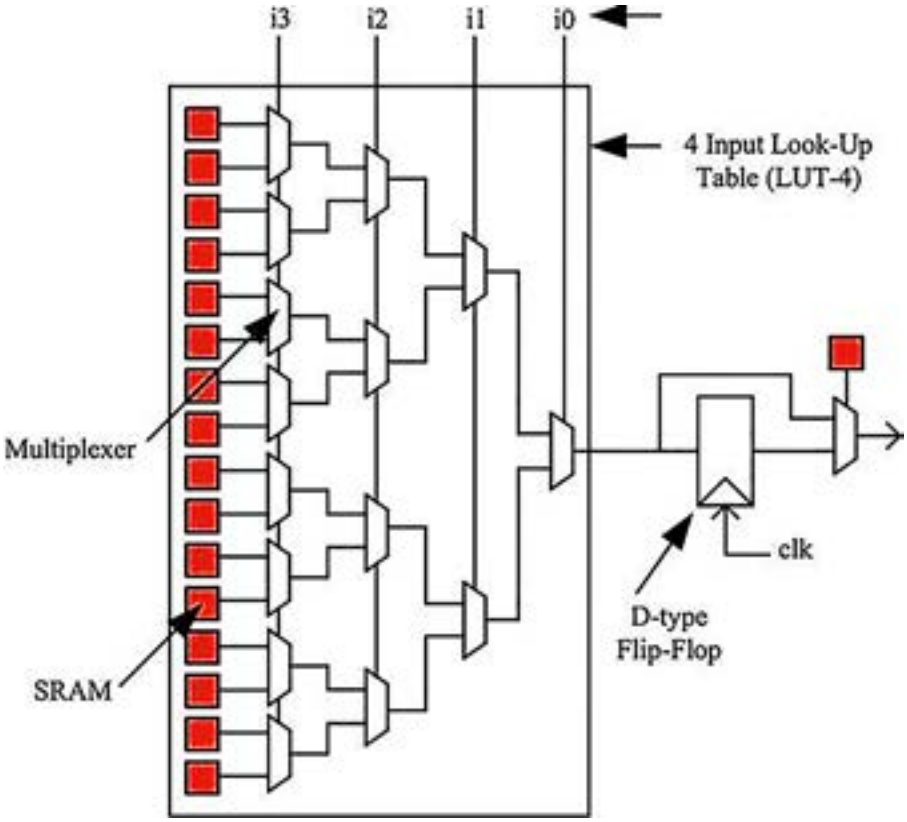


**Fig.2:** Basic Logic Element (BLE) [6]

## 1.2. Routing Resources

Routing resources consist of pre-fabricated wiring segments and programmable switches which are spread out around each logic cell vertically and horizontally. The organization of routing resources and Configurable Logic Block shown in Fig.3.

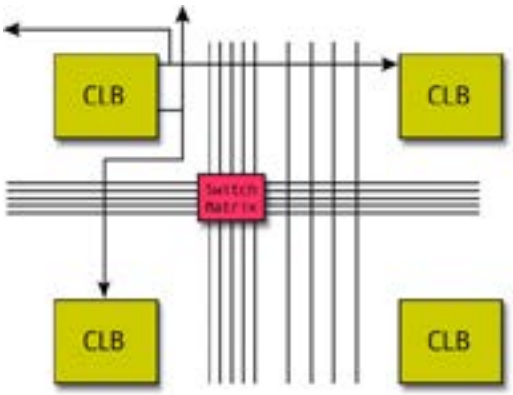


**Fig.3:** FPGA Routing Resource [7]

Fig.3 shows the interconnection between CLBs which is called global routing, where detailed routing provides miniscule information about switch Matrix [6]. Routing resources consumes maximum portion (almost 90%) of FPGA area and rest of the portion belongs to Logic blocks and I/Os [5]. That's why FPGAs are considered 18-35 (Area), 7-18 (Power) and 3-4 (Delay) times less efficient as compare to ASICs (Application Specific Integrated Circuits) [4].

## 1.3. Input / Output Blocks

Signals are going into the FPGA and move away from FPGA is due to Input/Output Block. It contains Input and output tristate buffer with collector open output [7] shown in fig.4. This block is also connected to routing interconnect [8].

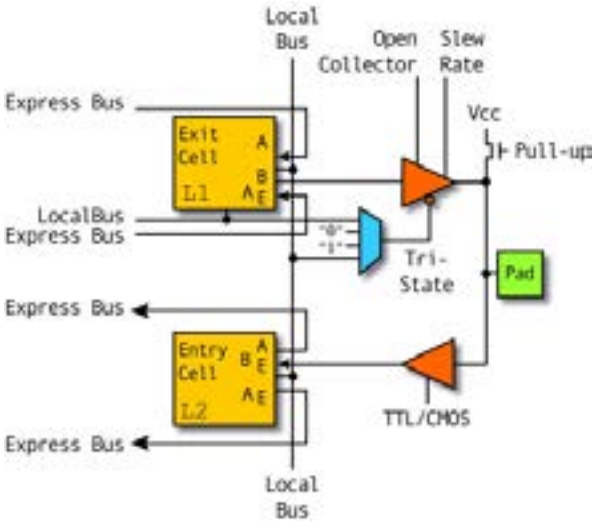


**Fig.4:** Input-Output Block [7]

## 2. Major Issues in FPGAs

### 2.1. Power Consumption in FPGAs

Optimizing power dissipation is one of most important factor in FPGA design. As number of transistor count per unit area is increased power dissipation of integrated Circuit is increased [16]. Sum of Static and Dynamic power is called total power. Static power is power dissipated at idle condition (inputs are inactive) where Dynamic power is more important because it continuously dissipates as signal switches because of capacitances (load/dependent) [17]. The expression is shown in (i):

$$P_{Dyn} = \sum_{Nodes} (0.5 * C_y * V^2 * D(y) * f \quad \text{.....(i)}$$

f= Clock frequency;
V= Applied Voltage;
$C_y$= Capacitance of node;
D(y)= Switching activity at each node;

Dynamic power depends linearly on clock frequency and quadratically on applied voltage [18,19]. Power dissipation in FPGA can be analyzed with the help of simulation which uses benchmark input stimuli to evaluate switching activity of desired circuit [20].

### 2.2. FPGA Area

FPGA area can be calculated by mapping a complete FPGA tile which describes routing and logic area [4]. Routing area is most important as it occupies almost 90% of total FPGA area [21] , routing area increased not due to wiring interconnect but it increases due to number of transistor per unit area. To measure accurate Area, authors in [21] introduced an area model based on measuring total number of transistors precisely. The area model is stated as function of λ which is equal to ½ of the minimum distance among drain and source terminal of transistor. They also found type of switches, wiring and Logic blocks used for specific connection with the help of routing resource graph. In reference [9], the authors developed an Area Model based on minimum width of Transistor shown in (ii):

$$\text{Area}(W) = (\beta + a * W/W_{Min}) \text{Area}_{MWTA} \quad \text{.....(ii)}$$

a, β and $\text{Area}_{MWTA}$ are process specific constants

### 2.3. FPGA Delay

It is very difficult to optimize FPGA delay because we are not able to calculate critical path (slowest path) at the time of design, as critical path is depending upon type of application circuits [22]. Performance of any employed circuit can be anticipated by evaluating its critical path [21]. Physical design and cell library of FPGA are responsible for wiring and switching delays. In reference [22], Delay is estimated by: i) Evaluating the delay for each component in the path. ii) Collect these delays calculations to generate an Aggregate delay. iii) Each component's delay has weight, depending upon how many times it is confronted with critical path of a benchmark circuit. In reference [21] highly accurate wires and switch delays estimation is obtained by using ELDO circuit simulator which is based on extracted layout parameters. So for different optimization techniques have been used to optimize Power, Area and delay tradeoffs. These techniques can be categorized as:

a. Improvement at Architectural Level such as cluster sizing, how many inputs are used per cluster and crossbar arrangement [8-10].
b. Improving performance by replacing traditional LUTs with highly proficient (in terms of Power, Area and delay) Logic block [13-15].
c. Optimizing placement and routing algorithms to improve FPGA design [11,12].

In the above section, FPGA architecture together with optimization techniques and their related parameters are discussed. In the next section, the existing work related to FPGA architecture issues related with power, speed, density of different FPGA architecture are discussed.

## 3. Detailed Review of Existing Techniques

There are various techniques have been proposed for addressing different issues related to FPGA routing, power consumption, mapping, LUTs and etc. The each FPGA used have different advantages and disadvantages for particular issue of FPGA. In the section, the important existing techniques have been discussed related to modern trade-off FPGA architecture. The Table 1, discussed the important aspects for modern trade-off FPGA architecture;

**Table 1:** Detailed Review of Existing Techniques

| S.N | Author (year) | Problem Statement | Solution | Technique |
|---|---|---|---|---|
| 1. | Behnam Khaleghi (2018) | SRAM blocks are not efficient in terms of Area and Power. Programming structure with large memory and low performance. | Efficient design of switch box and LUTs with improved programming by using RRAM based FPGA Architecture | Switch Box and LUTs are RRAM based Integrated with sequential programming scheme |
| 2. | Wenyi Feng, Jonathan Greene ( 2018) | Configuration bit cell area has not been keeping up with scaling | S44-structure input structure composed of two tightly coupled4-input LUTs | Re-synthesize and mapping |
| 3. | Rana Alhalabi (2017) | Speed of memory access lowers the execution speed in FPGAs. | To overcome this speed issue Nonvolatile Look up table is used. | Spin transfer torque magnetic RAM (STT-RAM) and Delay is reduced by separating CMOS MUX from read current path |
| 4. | Safeen Huda (2017) | Over provisioned with routing resources | Identify routing conductors that are not in use to control power. | Overall energy dissipation is improved by Using CAD techniques. |
| 5. | Zahra Ebrahimi (2017) | Logic integration in FPGA becomes restricted due to increase in static power | Using 3 input LUT, reconfigurable hard logic and soft logic. | Static power is minimized by turning off inactive hard and soft logic elements. |

| S.N | Author (year) | Problem Statement | Solution | Technique |
|---|---|---|---|---|
| 6 | Sonda CHTOUROU (2017) | Overall analysis to minimize Power, Area and delay tradeoff. | Novel Architecture by combining mesh and hierarchical topologies | Butterfly-fat-tree(BFT) topology |
| 7. | Xifan Tang (2017) | As number of input is increased delay in SRAM FPGA multiplexer increase linearly.. | To overcome this issue Enhanced RRAM FPGA architecture is used. | Increase Capacity of SB MUXes |
| 8. | Tao Luo (2017) | Improve FPGA design | FPGA design is improved by new CLB which consists of LUTs and Universal logic gates (ULGs). | To get the optimum solution, the ratio of ULGs and LUTs in CLB is explored by using benchmark circuits. |
| 9. | Ali Asghar (2016) | LUTs flexibility increases area overhead. As the LUT size increases amount of configuration memory grows exponentially. | Using CLBs with shared LUTs | A new clustering technique has been proposed which packs NPN equivalent functions together inside a Configurable Logic Block (CLB). |
| 10. | Iman Ahmadpour (2015) | Substantial flexibility of Look-Up Tables (LUTs) in implementing arbitrary functions comes with significant | First identify the most frequently used functions in standard Benchmarks. | We use the Shannon expansion to break 5-variable functions into two asymmetric functions, |

| S.N | Author (year) | Problem Statement | Solution | Technique |
|---|---|---|---|---|
| | | performance and area Limitations | Design a Hard Logics (HL) which is set of less-flexible but area-efficient logic cells. | wherein one of them has less than K -1 inputs. A mixed LUT-HL architecture and a mapping scheme are proposed to accomplish maximum logic resource usage. |
| 11 | Pierre-Emmanuel Gaillardon (OCT 15) | At advanced technology nodes, more and more devices are affected by Schottky contacts at the source and drain interfaces. Hence, devices face an ambipolar (exhibits n- and p-type characteristics simultaneously) behavior. | A Novel architectural organization in which standard lookup tables (LUTs) are replaced by ultrafine-grain Logic cells (LCs). | Build ultrafine grain computation cells, called MClusters. |
| 12. | Qian Zhao (2014) | As more configuration memory cells are embedded to improve FPGA Scale, larger area | Decreasing configuration memory by Implementing partial functions of Shannon | A novel SLM architecture which provides high logic coverage with less area and configuration |

| S.N | Author (year) | Problem Statement | Solution | Technique |
|---|---|---|---|---|
| | | and more power consumption is required resulting increase in soft-error rate per device. | expansion for recurrently appearing logics. | memory as compare to orthodox LUT. |
| 13 | Ian Kuon and Jonathan Rose (2011) | For different markets, FPGA area, performance and power are of different importance and closing one of the gaps could be essential. By exploring the tradeoffs possible the limits for FPGAs can be better understood since that will demonstrate the extent to which any of the gaps can be narrowed. | To understand the circuit and architectural design attributes of an FPGA that enable tradeoffs between area and speed, and to determine the magnitude of the possible trade-offs. | Varying both architecture and transistor sizing of an FPGA. A transistor-level optimization tool is used to explore these trade-offs and examine what we call the area-delay design space for FPGAs. |

Table 1 showed a different aspects of FPGA related issues, their solutions and techniques have been discussed. With the help of Table 1, detailed analysis of existing trade-offs in FPGAs is discussed to demonstrates the modern aspects of FPGA power, density and speed in optimization of FPGA.

## 4. Analysis over Power, Delay And Area Trade-Offs In Modern FPGA Architectures: Optimization Techniques

Khaleghi and Asadi [25] discussed the Non-Volatile Memories (NVMs) in Field Programmable Gate Arrays FPGAs. The authors define that as FPGAs are not developed enough to replace traditional SRAM based FPGA because Main blocks are not efficient in terms of Area, Power and Programming structure which consumes large memory and low performance. In response, the authors have proposed an efficient design of switch box and LUTs with improved programming by using Resistive RAM based FPGA Architecture. The LUTs in the

proposed model are capable of handling large number of inputs because it uses only two transistors for programming in conjunction with pass transistors and boosting buffers.

The static and dynamic power in proposed models are decreased by 24.3% and 56% respectively. Whereas speed and Area is decreased by 20.1% and 59.4%. Feng, Greene, and Mishchenko [26] define the Impact of advancing technology is that configuration bit cell area has not been keeping up with scaling. From 150nm to16nm a shrink of 88x would be expected but SRAM FPGA Configuration bit cell area has shrunk by only about 36x. The authors have solved the issue using "S44" structure, 7-input structure composed of two tightly coupled 4-input LUTs. The solution have been demonstrated using re-synthesize and mapping (using ABC), packing, placement and routing. The authors further discussed the use of a modified version of the Libero Design Suite. In response of the designed system, the FPGA of 14nm consumes, static power tends to correlate with area 134.7(ns) with total Delay of 15.6% area saving.

Alhalabi et al. [28] discussed that Speed of memory access lowers the execution speed in FPGAs and the overall function is affected by large amount of data. To overcome this problem a nonvolatile Lookup table based on Spin transfer torque magnetic RAM (STT-RAM) is employed. This nvLUT is also capable of handling large number of inputs. The overall area is significantly reduced by implemented N-MOS based pass gates. The power consumption is reduced up to 46%, and speed delay is reduced up to 55%, and density area of 47% reduced is for the designed FPGA based system shown in fig 5.

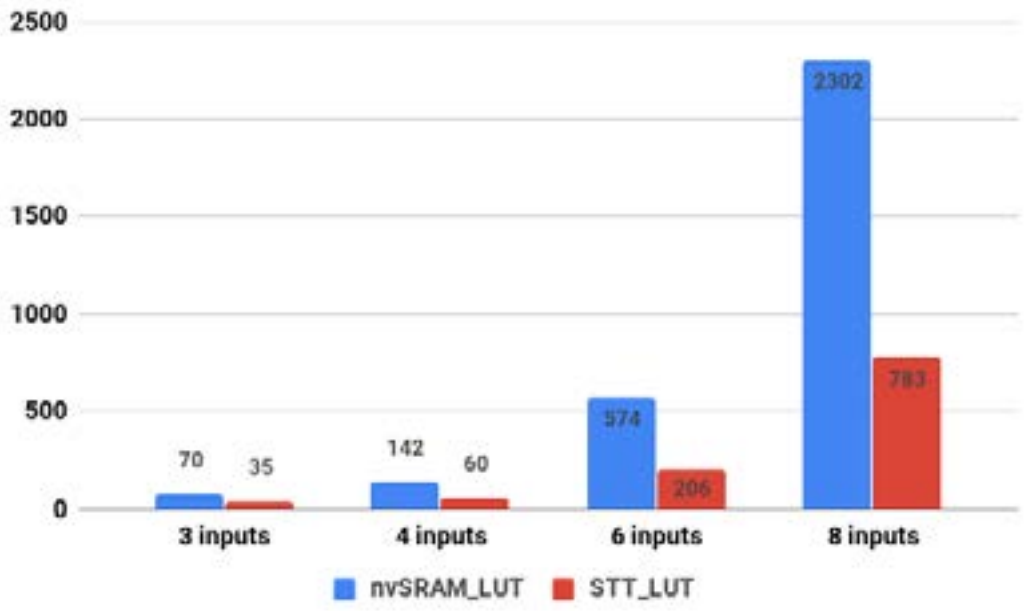


**Fig.5:** Comparison of density area (number of Transistors) [28]

Huda and Anderson [27] discussed that, Routing power in FPGAs is increased significantly due to the routing resources, as they occupy most of the FPGA Area. The authors define that dynamic power can be controlled by identifying routing conductors that are not in use and static power can be reduced by observing leakage in routing multiplexers. To optimize total power consumption in routing network CAD tools are used. Results show that dynamic and static power are reduced up to 25% and 81% respectively and delay speed of 10% with delay overhead over of area-overhead of 2.6%–4.8%.

Ebrahimi, Khaleghi and Asadi [23] discussed about the SRAM FPGA based architectures. For existing and future technologies Logic integration in FPGA becomes restricted due to increase in static power. They proposed an FPGA Architecture which is efficient in power. It is based on combination of three input LUT with reconfigurable hard logic with soft logic. The authors use power gating technique in which Static power of logic blocks is minimized by turning off inactive hard and soft logic elements. In response, the 24.5% Static Power, dynamic power 39.7 % and speed delay of 21.3% with approximate 19% area is reduced using the proposed technique shown in Table 2.

**Table 2:** Combined Results by all benchmarks [23]

| **Parameter/Architecture** | **PG 4-LUT** | **6-LUT** | **PG 6-LUT** | **[26]** | **PEAF** |
|---|---|---|---|---|---|
| Logic Delay | 1.07 | 0.85 | 0.91 | 0.73 | 0.80 |
| Routing Delay | 1.00 | 0.88 | 0.88 | 1.06 | 1.17 |
| **Total Delay** | 1.03 | 0.86 | 0.87 | 0.89 | 0.98 |
| Logic Static Power | 0.81 | 1.64 | 1.25 | 0.72 | 0.43 |
| Routing Static Power | 1.00 | 0.96 | 0.96 | 1.05 | 1.11 |
| **Total Static Power** | 0.90 | 1.31 | 1.09 | 0.88 | 0.81 |
| Logic Dynamic Power | 1.00 | 1.92 | 1.92 | 0.73 | 0.64 |
| Routing Dynamic Power | 1.00 | 1.23 | 1.23 | 1.15 | 1.04 |
| **Total Dynamic Power** | 1.00 | 1.49 | 1.49 | 0.99 | 0.90 |
| Logic Total Power | 0.82 | 1.64 | 1.26 | 0.72 | 0.44 |
| Routing Total Power | 1.00 | 0.97 | 0.97 | 1.05 | 1.10 |
| **Total Power** | 0.90 | 1.31 | 1.11 | 0.88 | 0.81 |
| Logic Area | 1.02 | 1.85 | 1.87 | 1.31 | 1.21 |
| Routing Area | 1.00 | 1.20 | 1.20 | 1.11 | 1.17 |
| **Total Area** | 1.01 | 1.40 | 1.41 | 1.21 | 1.19 |
| **PDP** | 0.92 | 1.13 | 0.96 | 0.82 | 0.78 |

Chtourou et al. [21] performed an overall analysis to minimize Power, Area and delay tradeoffs. The authors introduced a novel architecture by joining mesh and hierarchical topologies. They employed butterfly fat tree (BFT) topology which based on unoccupied routing interconnection. By implementing proposed architecture authors conclude that: Power dissipation, delay, and area are 205nw, 55.255(ns) and 17500(E+6λ2) respectively with optimum cluster size is 8 and LUT size is 4. The area density of 17500 (E+6λ2) with Best cluster size 8 and LUT size 4 is achieved using the proposed technique shown in fig.6-8.

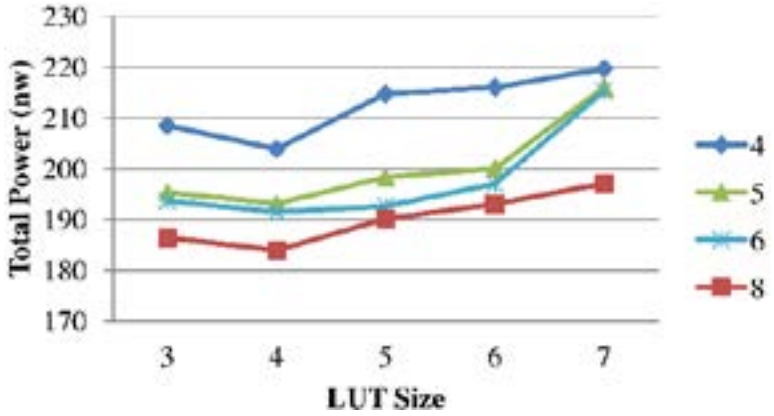


**Fig.6:** Total power versus LUT size [21]

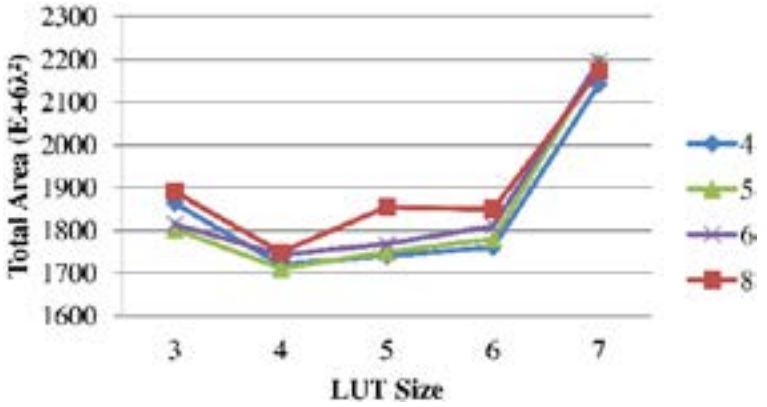


**Fig.7:** Total Area versus LUT size [21]

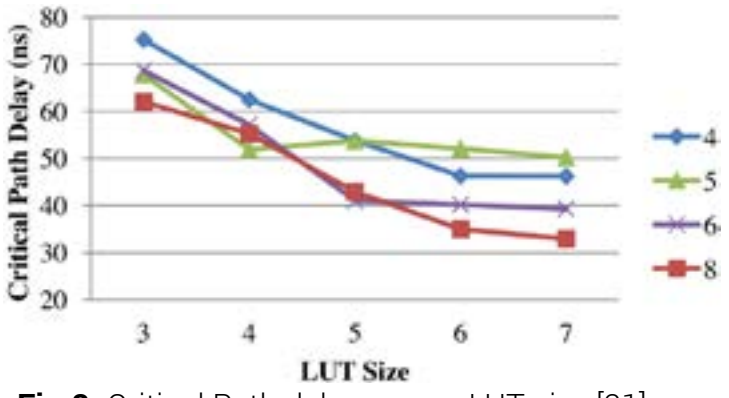


**Fig.8:** Critical Path delay versus LUT size [21]

Tang, De Micheli and Gaillardon [24] define the delay of SRAM FPGA multiplexers, as number of inputs increased delay in SRAM FPGA multiplexer increase linearly. Due to this constraint, SRAM FPGAs are bound to use small crossbars to control power, area and delay tradeoff. To solve this issue, they suggested a new Resistive RAM based FPGA architecture with three architectural enhancements. It uses larger multiplexer containing single level crossbars. Integrated connection box improves capacity of switch box multiplexers. The Smaller Best Length Wire < 4 20%-58% power saving of 45%-58% performance improvement, and 7%-15% area reduction is recorded using the proposed research work.

Luo et al. [29]'s FPGA design is improved by new CLB, which consists of LUTs with Universal logic gates. Proposed an improved FPGA architecture to optimize Power speed and density tradeoffs. Optimal results have been achieved by incorporating a new type of CLB, which is combination of universal logic gates (ULGs) and Lookup tables (LUTs). The most important task is to find the appropriate ratio of ULGs and LUTs in CLB, which is resolved by performing detailed investigation on benchmark circuits. The authors save power up to 17.1% and speed up to 11.2% and density up 10.4%.

Asghar et al. [15] explored how LUTs flexibility (to perform every possible Boolean function) increases area overhead which results exponential growth in configuration Memory. To overcome this problem, the authors proposed a novel FPGA architecture which allows sharing of LUTs SRAM routes between NPN equivalent functions. By implementing this technique they achieved reduction of 30% configuration memory cells of logic blocks ,which results 3.7% of area with critical path delay of less than 1%.

Gaillardon et al. [30] discussed that, as technology advances devices are affected by "Schottky contacts" which causes ambipolar characteristics. Author introduced a new architecture arrangement in which tradition LUTs are substituted by ultra-fine grain logic cells, resulting computation cells are called MClusters. In the proposed architecture the polarity of transistor is controllable with electrostatic programming. Experimental results discovered that dynamic power is reduced by 54%.as compare to CMOS FPGA 23% as compare to CMOS FPGA and 43% as compare to CMOS FPGA is achieved using the proposed work.

Ahmedpour, Khaleghi and Asadi [31] discussed how Substantial flexibility of Look-Up Tables (LUTs) in implementing arbitrary functions results significant performance and area Limitations. They proposed a mixed LUT-HL(Hard Logics which is set of less-flexible but area-efficient logic cells) architecture and a mapping scheme to accomplish maximum logic resource usage. MCNC Benchmarks reveal that the proposed architecture

improves performance by 17% and 2% as compared to LUT4 and LUT6 based FPGAs. Reduces area-delay product by 13% and 36% as compared to LUT4 and LUT6 based FPGAs.

Zhao et al. [32] revealed as more configuration memory cells are embedded to improve FPGA Scale, larger area and more power consumption is required resulting increase in soft-error rate per device. He reduced configuration memory by implementing partial functions of is achieved using the proposed technique. Shannon expansion for recurrently appearing logics. He proposed A novel SLM (Scalable Logic Module) architecture which provides high logic coverage with less area and configuration memory as compare to conventional LUT. Experimental results shows that 7-SLM and 8-SLM occupy 20.74% and 28.95% less area as compare to 7 and 8 LUTs respectively whereas the area delay product for 7-SLM FPGA is better than all the LUT FPGAs.

Kuon and Rose [22] evaluated the magnitude of power, speed and density tradeoffs in FPGAs. The authors explored the extent of tradeoffs by varying architecture and transistor size of an FPGA. "Automated transistor design tool" was implemented to get the optimum range of trade-offs. They discovered that Power dissipation is strictly related to area and by varying the architecture along with the transistorizing, area varied by a factor of 2.0.

In this section, various techniques have been proposed based on analysis over Power, delay and Density Tradeoffs in Modern FPGA Architectures. In the next, conclusion is discussed about the latest Trade-offs in Modern FPGA Architectures in Optimization Techniques in terms of Power, Speed and Density.

## 5. Conclusion

In this paper various techniques to optimize Power, density and speed tradeoffs have discussed. We explored that Dynamic power is reduced by 56% , static power is decreased by 24.3% , speed is improved by 20.1% and density is improved by 59.4% by using Resistive RAM based FPGA architecture [25]. It is also discussed that discussed that using "S44" structure, area 134.7(ns) with total Delay of 15.6% area saving is achieved. Power saving up to 46%, and speed delay is reduced up to 55%, and density area of 47% reduced when Spin transfer torque magnetic RAM (STT-RAM) based FPGA system is employed [26]. When CAD tools are used in routing network it yields that dynamic and static power are reduced up to 25% and 81% respectively, the delay speed of 10% with delay overhead over of area-overhead of 2.6%–4.8% [27]. When architecture with combination of three input LUT,

reconfigurable hard logic and soft logic is used it gives the 24.5% Static Power, dynamic power 39.7 % and speed delay of 21.3% with 18.9% overhead [23]. It has been defined that overall, in existing work the maximum reduction in delay speed is achieved is of 58% [24] and maximum reduction in power consumption is achieved is of 81% [27], and maximum reduction in area density is achieved is of 59.4% [25] and the area delay product for 7-SLM FPGA is better than all the LUT FPGAs [32].

However, it has been analyzed from the discussed FPGA architectures and optimization techniques that still there is a lot of improvement needed in order to make energy efficient Trade-offs in Modern FPGA Architectures in terms of Power, Speed and Density. There are various areas in this direction are still need to be explored more such as; I/O Placement Locking, Timing-Driven Packing and Placement, Place and Route, Pipelined Floating-Point Exponential Unit Machine learning based methods to predict routing congestion ,and many more. In the future, the above discussed area need to be explored in order to optimize the power, density, and speed delay for discussed FPGA architectures for different issues.

## Reference


1. M. M. Iqbal and H. Parvez "Optimizing Routing Network of Shared Hardware Design for Multiple Application Circuits," in Proc. of the First International Conference on Latest trends in Electrical Engineering and Computing Technologies (INTELLECT), 2017,pp. 1 – 4.
2. V. Betz and J. Rose, "Cluster-Based Logic Blocks for FPGAs: Area Efficiency vs. Input Sharing and Size," In Proc. of the CICC, 1997, pp. 551-554.
3. S. Akthar. "All about FPGA," Internet: https://allaboutfpga.com/fpga-architecture/, April 16, 2014 [24 Jan 2019].
4. I. Kuon and J. Rose, Quantifying and exploring the gap between FPGA and ASICs. *Springer Science and Business Media,2010.*
5. V. Betz, J. Rose, and A. Marquardt, Architecture and CAD for Deep-Submicron FPGAs. New York, NY, USA: Kluwer, 1999.
6. U. Farooq et al., *Tree-Based Heterogeneous FPGA Architectures*, Springer Science and Business Media, New York 2012.
7. B. Zeidman, "All about FPGAs". Internet: https://www.eetimes.com/document.asp?doc_id=1274496 , March 22, 2006 [10.10.18]
8. V. Betz and J. Rose, "How much logic should go in an FPGA logic block", IEEE

Design & Test of Computers, Vol. 15, no. 1, pp. 1015,1998.

9. E. Ahmed and J. Rose, "The effect of LUT and cluster size on deep-submicron FPGA performance and density", in *Proc*. of the *ACM/SIGDA* 8th *International Symposium* on FPGAs, 2000.
10. A. DeHon, "Balancing Interconnect and Computation in a Reconfigurable Computing Array (or, why you do not really want 100% LUT utilization)", in *Proc*. of the *ACM/SIGDA* 7th I*nternational Symposium on FPGAs*, Monterey, CA, USA, 1999.
11. Parvez, H., Marrakchi, Z., and Mehrez, H. "ASIF: Application specific inflexible FPGA". In *Proc. of the International Conference on Field Programmable Technology (ICFPT09),* 2009.
12. M.M. Iqbal and H. Parvez. "Multi-Circuit": Automatic Generation of an Application Specific Configurable Core for Known Set of Application Circuits." *Journal of Circuits, Systems, and Computers*. Vol. 25, No. 9, 2016.
13. Y. Okamoto et al. "COGRE: a configuration memory reduced reconfigurable logic cell architecture for area minimization," In *Proc*. of the *International Conference on Field Programmable Logic and Applications*, 2010, pp. 304309, 2010.
14. B. K. I. Ahmadpour and H. Asadi, "An efficient reconfigurable architecture by characterizing most frequent logic functions", in Proc. of the *25th International Conference on Field Programmable Logic and Applications (FPL)*, 2015, pp. 1 - 6.
15. A. Asghar, M. M. Iqbal, W. Ahmed et al., "Exploring shared SRAM tables among NPN equivalent large LUTs in SRAM based FPGAs", in *Proc. of the International Conference on Field Programmable Technology (ICFPT),* 2016, pp. 229232 .
16. Lattice Semiconductor, "Power considerations in FPGA design", Internet: http://www.latticesemi.com/-/media/LatticeSemi/Documents/WhitePapers/NZ/PowerConsiderationsinFPGADesignLatticeECP3.ashx?document_id=32410, February 2009.
17. S. Chtourou et al., "Power dissipation analysis for island-style FPGA architecture", in *Proc. of the 5th International Conference on Information and Communication Systems (ICICS),* 2014,pp. 1 – 4
18. D. Eckerbert and P. Larsson-Edefors, "Interconnect-Driven Short-Circuit,Power Modeling, in *Proc*. of the *Euromicro Symposium on Digital Systems Design*, 2001, pp. 412-421.
19. Q. Wang and S.B.K. Vrudhula, "On Short Circuit Power Estimation of CMOS Inverters", in Proc. of the *IEEE International Conference on Computer Design (ICCD),* 1998, pp. 70-75.

20. L. Shang, A. S. Kaviani, and K. Bathala," Dynamic power consumption in Virtex-II FPGA family". *in Proc. of the ACM/SIGDA Tenth International Symposium on Field-programmable Gate Arrays*, 2002, pp. 157–164,.
21. Sonda CHTOUROU, Zied MARRAKCHI, Emna AMOURI,Vinod PANGRACIOUS, Mohamed ABID, Habib MEHREZ and Habib MEHREZ "Performance analysis and optimization of cluster-based mesh FPGA architectures: design methodology and CAD tool support", *Turkish Journal of Electrical Engineering & Computer Sciences, 2017 Vol 25: 2044-2054.*
22. I. Kuon and J. Rose, "Exploring Area and Delay Tradeoffs in FPGAs With Architecture and Automated Transistor Design" I*EEE Transactions on Very Large Scale Integration (VLSI) Systems,* 2011, Vol. 19, Issue: 1, pp. 71 – 84.
23. Z. Ebrahimi, B. Khaleghi, and H. Asadi, "PEAF: A power-efficient architecture for SRAM-based FPGAs using reconfigurable hard logic design in dark silicon era," *IEEE Trans. Comput*., Vol. 66, no. 6, 2017, pp. 982–995.
24. X.Tang, G.i De Micheli and P. Gaillardon "Optimization Opportunities in RRAM-based FPGA Architectures", in *Proc.* of the IEEE *8th Latin American Symposium on Circuits & Systems (LASCAS),* 2017.
25. B. Khaleghi and H. Asadi "A Resistive RAM-Based FPGA Architecture Equipped With Efficient Programming Circuitry", *IEEE Transactions on Circuits and Systems I: Regular Papers,* Vol.: 65, Issue: 7, 2018, pp. 2196 – 2209.
26. W. Feng, J.Greene and A. Mishchenko," Improving FPGA Performance with a S44 LUT Structure" in *Proc,* of the 2018 *ACM/SIGDA International Symposium on Field-Programmable Gate Arrays,* 2018, pp. 61-66.
27. S. Huda and J.H. Anderson, "Leveraging Unused Resources for Energy Optimization of FPGA Interconnect", *IEEE Transactions on Very Large Scale Integration (VLSI) Systems Year:* 2017, Vol. 25, Issue 8, pp. 2307 – 2320
28. R. Alhalabi et al. " High speed and high-area efficiency non-volatile look-up table design based on magnetic tunnel junction", in *Proc. of the 17th Non-Volatile Memory Technology Symposium (NVMTS),* 2017,pp. 1 – 4.
29. T. Luo et al. "A Hybrid Logic Block Architecture in FPGA for Holistic Efficiency", *IEEE Transactions on Circuits and Systems II: Express Briefs,* Vol. 64, Issue 1, 2017, pp. 71 – 75.
30. P. Gaillardon et al., "A Novel FPGA Architecture Based on Ultrafine Grain Reconfigurable Logic Cells", *IEEE Transactions on Very Large Scale Integration*

*(VLSI) Systems*, Vol. 23, Issue 10, 2015, pp. 2187 – 2197.

31. I. Ahmadpour, B. Khaleghi, and H. Asadi, "An Efficient Reconfigurable Architecture by Characterizing Most Frequent Logic Functions", in *Proc*. of the *25th International Conference on Field Programmable Logic and Applications (FPL),* 2015, pp. 1 – 6.
32. Q. Zhao et al. "A logic cell architecture exploiting the Shannon expansion for the reduction of configuration memory", in *Proc*. of the *24th International Conference on Field Programmable Logic and Applications (FPL), 2014, pp 1 - 6.*